Transition to Lead-free Electronics Assembly
Case Study

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Introduction

There are numerous factors that drive companies in the electronics industry to switch to less hazardous materials in their products. These factors can be categorized as regulatory and market drivers. For regulatory drivers, the European Union has enacted several directives over the past several years aimed at restricting the use of certain hazardous materials in electrical and electronic equipment. In January 2003, The European Union (EU) published directives on Waste Electrical and Electronic Equipment (WEEE) and the Restriction of Hazardous Substances (RoHS) in electrical and electronic equipment.

The WEEE directive deals with end-of-life management of electrical and electronic equipment (e.g., take-back and recycling of used computers and equipment), whereas the RoHS directive addresses types of materials used in manufacturing electrical and electronic equipment. RoHS restricts the following six chemicals above certain threshold amounts, with certain exceptions: lead, cadmium, hexavalent chromium, mercury, poly-brominated biphenyls and poly-brominated diphenyl ethers, with a target implementation date of July 1, 2006. Companies that sell products in the European Union must find safer alternatives for these substances to continue selling into the European marketplace.

Even in the absence of regulatory requirements, many large companies have responded, to a lesser extent, to market drivers and taken the initiative to eliminate materials of concern from their products where possible. They are trying to make more environmentally friendly and recyclable products, as well as trying to phase out materials they believe may be restricted in the future. These requirements move down the supply chain to manufacturers worldwide, who must be able to supply components without these materials or risk loss of business.

In January 2006, Benchmark Electronics conducted a lead-free implementation for one of its existing customers, Mercury Computer Systems of Chelmsford, MA. The lead-free implementation was conducted on an existing printed wiring board assembly used for medical equipment. Benchmark Electronics Hudson, NH division has been manufacturing this board using tin/lead solder paste for the past several years.

Mercury requested Benchmark Electronics Hudson, NH division to assemble the board using lead-free solder paste, lead-free board surface finish, and lead-free component finishes. Although this specific product is exempt from the upcoming RoHS directive for lead-free electronics, there is tremendous value in conducting this lead-free transition in advance of possible end-user mandates or changes in the RoHS product exemptions. By conducting this early transition, the issues and challenges of transitioning to lead-free electronics assembly can be identified and addressed in the most cost-efficient manner.

Mercury will conduct reliability testing for this lead-free board assembly subsequent to the writing of this paper. It is anticipated the reliability testing results will be made publicly available as an addendum to this paper.

Printed Wiring Board

The printed circuit board has a footprint of approximately 7.5 x 9.2 inches. The board is 16 layers and has a thickness of 84 mils. The laminate material chosen to meet the higher thermal requirements for the lead-free assembly is the Isola IS410 product. This product has a glass transition temperature of 180 degrees C and is specially formulated for high performance through multiple thermal excursions.

The board is populated with 1,694 components on the top and bottom sides. The components include both surface mount (e.g. ball grid arrays [BGAs], Small Outline ICs (SOICs), discretes, etc.) and through-hole technology (i.e. connectors). This includes 15 lead-free BGAs on the bottom side, and 11 lead-free BGAs on the top side. Figure 1 shows the completed printed wiring board.

Figure 1. Printed Wiring Board.

Component Availability

In order for components to be acceptable for lead-free assembly, they must have both a lead-free component finish and the ability to withstand the higher temperature profiles of lead-free processing. Of the 1,694 components, 1,675 were available that met those two requirements. The remaining 19 components were missing these requirements as outlined in Table 1.

Table 1. Lead-Free Assembly Components

Number of Components	Lead-free Component Finish	Can Withstand the Lead-free Temperature Profile
1,675	Yes	Yes
14 (BGAs)	No	No
5 (ICs)	No	No

The 19 components were either not available with a lead-free finish, or it was cost prohibitive for the vendor to change the component to a lead-free finish. For example, the vendor of one of the tin/lead BGAs requested a charge of $600,000 to change one lot of its BGAs to lead-free.

Upon completion of a review of component supplier data, only 13 BGAs were considered to be tin/lead. However, upon conducting X-ray Fluorescence (XRF) scans during incoming quality inspection, it was discovered that a BGA that was claimed to be lead-free actually contained tin/lead solder. Consequently, the number of BGAs without lead-free solder was increased to 14.

Assembly Process

For the 19 components that did not meet these lead-free requirements, special processing was needed. The special processing options considered for the 14 BGAs included: reballing the BGAs with lead-free balls, using an Air-Vac rework machine, or microstenciling. Each of these options would have an impact on potential reliability issues, process cost increases, and process-cycle-time increases. Microstenciling was determined to have the smallest overall impact, and therefore the 14 BGAs were micro-stenciled and then sent to the reflow oven for the tin/lead profile. This included eight BGAs on the bottom side, and six BGAs on the top side. Consequently, four reflow passes were required in total to accommodate all the SMT components. The five ICs were hand soldered with tin/lead solder paste. Therefore, the sequence of the major steps for the board assembly was as follows:

1. Tape off 19 component locations on the stencil
2. Bottom side print and placement of SMT components
3. Bottom side reflow with lead-free profile (first pass)
4. Top side print and placement of SMT components
5. Top side reflow with lead-free profile (second pass)

6. Micro stencil bottom side and placement of eight BGAs
7. Bottom side reflow with tin/lead profile (3rd pass)
8. Micro stencil top side and placement of six BGAs
9. Top side reflow with tin/lead profile (4th pass)
10. Hand solder five ICs
11. Solder through hole components on Premier rework machine

The lead-free profile use for the first and second passes was a ramp to peak profile. The target peak temperature range was 240 – 248 degrees Celsius, and the target time above liquidus was 60 – 90 seconds. Figures 2 and 3 show the actual temperature profiles for the top and bottom side of the lead-free boards.
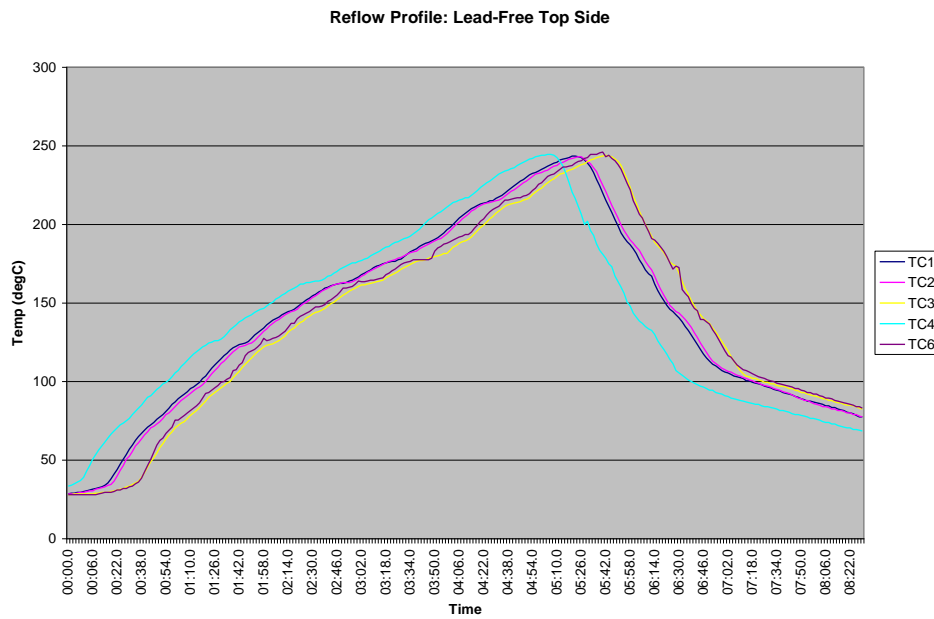

Figure 2. Reflow Profile – Lead-Free Top Side.
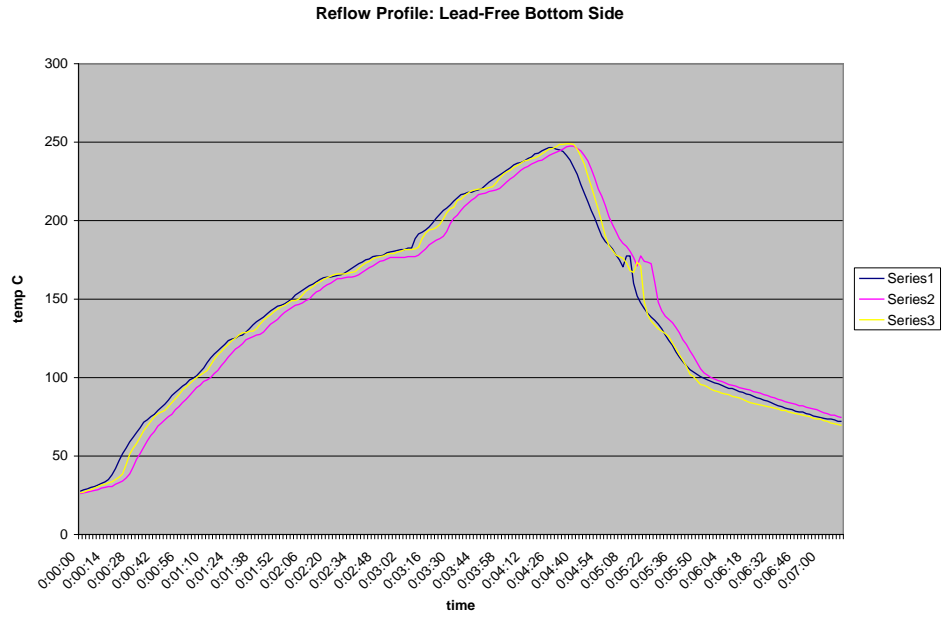
Reflow Profile: Lead-Free Bottom Side

Figure 3. Reflow Profile: Lead-Free Bottom Side.

The tin/lead profile used for the third and fourth passes also had a ramp to peak profile. The target peak temperature range was between 200 – 208 degrees Celsius. This peak temperature was sufficiently below 217 degrees Celsius to avoid the unintentional reflow of the lead-free components that had previously been assembled during the 1st and 2nd reflow passes. The target time above liquidus was 60 – 90 seconds. Figures 4 and 5 show the actual temperature profiles for the top and bottom side of the tin/lead boards.
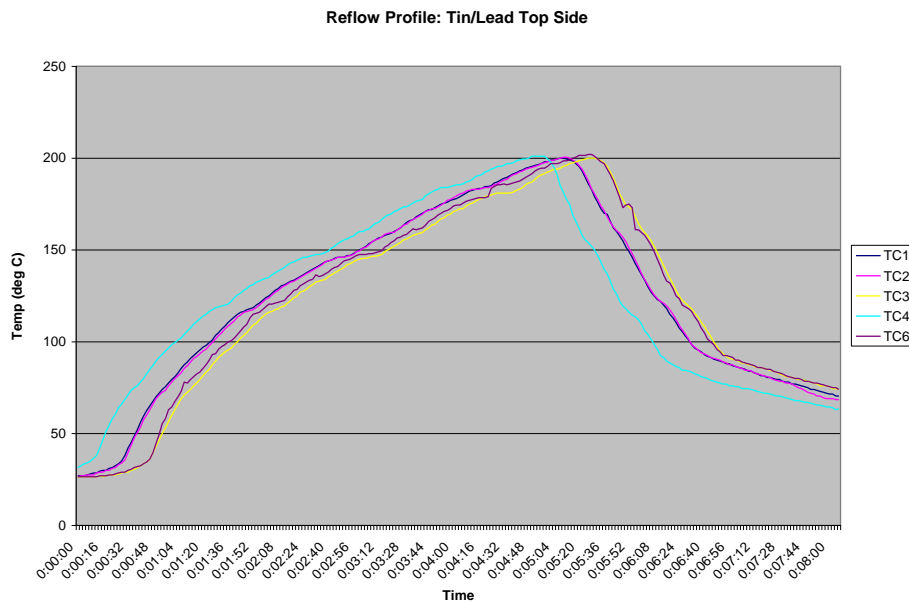
Reflow Profile: Tin/Lead Top Side

Figure 4. Reflow Profile: Tin/Lead Top Side.
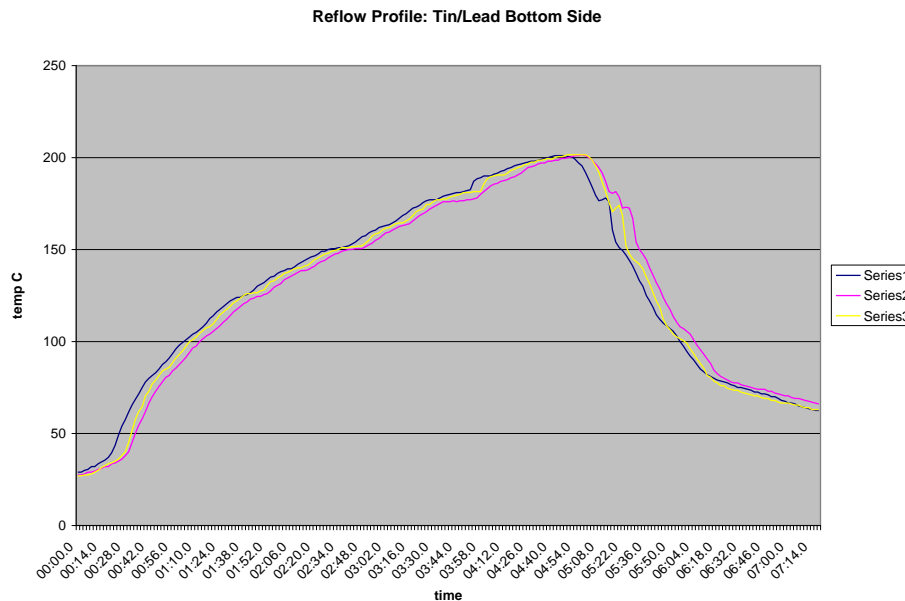
Reflow Profile: Tin/Lead Bottom Side

Figure 5. Reflow Profile: Tin/Lead Bottom Side.

Printing Process

For the tin/lead process, a water soluble solder paste was used. The lead-free water soluble solder pastes were selected based on extensive lead-free printing experiments previously conducted by Benchmark Electronics. The top-performing solder paste was used for the top side of the lead-free boards, and the second-highest performing solder paste was used for bottom side of the lead-free boards. During the experiment, there was some lot-to-lot variation in the performance of the second-highest performing solder paste. Therefore, printing validation tests should be considered when using different lots of solder paste.

The stencil used for assembling the tin/lead boards for the past few years is stainless steel and laser cut. The stencil is 6 mils thick and utilizes a 10% standard reduction for tin/lead assembly. This stencil will be referred to as "tin/lead stencil design."

A new stencil was fabricated to improve the printing process and appearance of the solder joints for lead-free electronics assembly. This stencil is also stainless steel laser cut, and 6 mils thick. However, the aperture sizes were changed to account for the different wetting properties of lead-free solder. For leaded devices and discrete components, aperture expansions were used in length, and a 1-to-1 pad-to-aperture ratio was used for the width. For the fine pitch devices, the aperture dimensions were based on pad size. The exact expansions and aperture dimensions used for the lead-free stencil is considered proprietary information. This stencil will be referred to as "lead-free stencil design."

A DEK printer was used for the lead-free boards. A 12-inch stainless steel blade was used with a front and rear pressure of 18.1 pounds. The print speed used for the first board was

0.9 inches per second. However, there was some incomplete pad coverage on the trailing edge of the larger pads. Consequently, the print speed was adjusted to 0.6 inches per second to provide complete pad coverage.

Through-hole Component Soldering Process
The through-hole components were assembled using a Premier rework machine. The lead-free solder used was the SAC 305 alloy, and the pot temperature was 285 degrees Celsius. The boards were preheated to 120 degrees Celsius, and the typical dwell time for soldering was 9 to 11 seconds.

Testing and Inspection
Various testing and inspection efforts were conducted for the 18 lead-free boards. In total, 65 defects were identified.

Automated Optical Inspection
During automated optical inspection, 17 defects were identified for the top side, and 30 defects for the bottom side. The defect types identified included: missing components, reversed components, damaged components, tombstoning, insufficient solder, solder bridge, and unsoldered leads.

Post Inspection
During post inspection, three defects were identified including missing component, component misregistered, and insufficient solder.

Continuity Test
A continuity test was conducted to check for any power-to-ground shorts prior to applying power. During the continuity test, one defect occurred due to a solder bridge.

Functional Test
A functional test was included to conduct communication tests. During the functional test, cache failures were identified due to two components with insufficient solder, one component with unsoldered leads, and one PCB continuity failure.

Burn-in Test
A burn-in test was conducted while the boards were in a 50 degrees Celsius environment for six hours. During the burn-in test, cache failures occurred due to six components with unsoldered leads.

Sun Test
The Sun test is a system test that is controlled using an automated software system. During the Sun test, there was an auto boot failure that required replacing two components.

Other Testing and Inspection
No defects were identified during the following testing and inspection efforts: final inspection, HP laminography, post touchup, third reflow inspection, fourth reflow inspection, and various X-ray inspections.

Design of Experiments – Lead-free Boards

A full factorial design was used to evaluate the influence of two factors on the quality of the lead-free boards: board surface finish and stencil design. Three levels were used for surface finish: organic solderability protectants (OSP), immersion silver, and electroless nickel immersion gold (ENIG). Two levels were used for stencil design: tin/lead stencil design, and lead-free stencil design. Therefore, there were six unique treatment combinations. Three replicates were used for each treatment combination for a total of 18 runs. The response variable is the number of defects identified for each board. To achieve randomization, the nine boards with a tin/lead stencil were assembled in random order, and then the nine boards with the lead-free stencil were assembled in random order.

Table 2 illustrates the factorial design, as well as the number of total defects identified during the testing and inspection process for the 18 lead-free boards.

Table 2. Lead-Free Boards Testing & Inspection Process

Board Number	Surface Finish	Stencil	Total Defects
1	OSP	Tin/Lead	7
2	OSP	Tin/Lead	2
3	OSP	Tin/Lead	1
4	OSP	Lead-free	7
5	OSP	Lead-free	5
6	OSP	Lead-free	5
7	Imm. Ag	Tin/Lead	1
8	Imm. Ag	Tin/Lead	2
9	Imm. Ag	Tin/Lead	3
10	Imm. Ag	Lead-free	1
11	Imm. Ag	Lead-free	4
12	Imm. Ag	Lead-free	5
13	ENIG	Tin/Lead	3
14	ENIG	Tin/Lead	2
15	ENIG	Tin/Lead	4
16	ENIG	Lead-free	6
17	ENIG	Lead-free	4
18	ENIG	Lead-free	3

Figure 6 illustrates the mean defect level per board for the three board surface finishes, and the two stencil types.
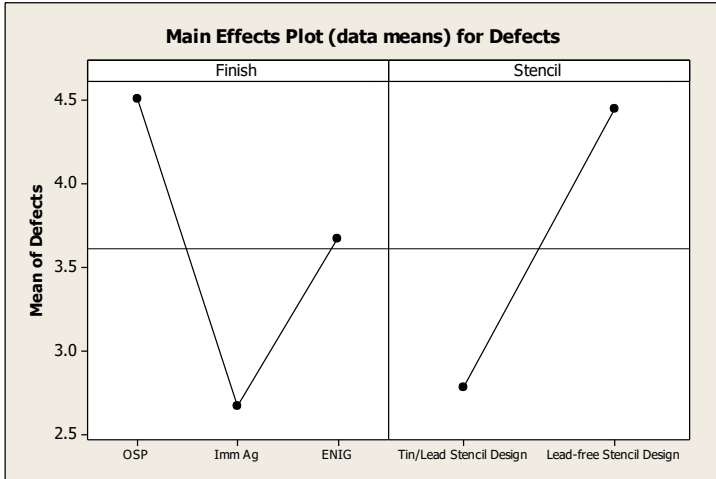
Figure 6. Main Effects Plot for Defects.

Figure 7 illustrates the interaction effect between the board surface finish and the stencil design. Since the lines are approximately parallel and there is no intersection, the interaction effects are not considered to be significant.

Figure 7. Interaction Plot for Defects.

The null hypothesis used for this experiment is that the expected number of defects for different treatments combinations within the experimental design will be the same. The alternative hypothesis is that the expected number of defects for different treatment combinations within the experimental design will not be the same.

A probability (p-value) is a measure of how much evidence we have against the null hypotheses. The smaller the p-value, the more evidence we have against the null hypothesis. For this experiment, we will reject the null hypothesis if the p-value is less than 0.05.

The following information is the Analysis of Variance for Defects, using Adjusted Sum of Squares for Tests. Since the probability is greater than 0.05 for the surface finish, stencil, and interaction effect, the null hypothesis should not be rejected. In other words, there is no statistical difference between the quantity of defects found between the boards based on board surface finish, stencil design, or any interactions of these two factors. Further evidence for this conclusion will be shown in subsequent confidence interval figures.

Table 3. Analysis of Variance for Defects

Source	Degrees of Freedom	Sequential Sum of Squares	Adjusted Sum of Squares	Adjusted Mean Square	F Value	Probability
Finish	2	10.11	10.11	5.06	1.49	0.264
Stencil	1	12.5	12.5	12.5	3.69	0.079
Finish*Stencil	2	1.0	1.0	0.5	0.15	0.864
Error	12	40.67	40.67	3.39		
Total	17	64.28				

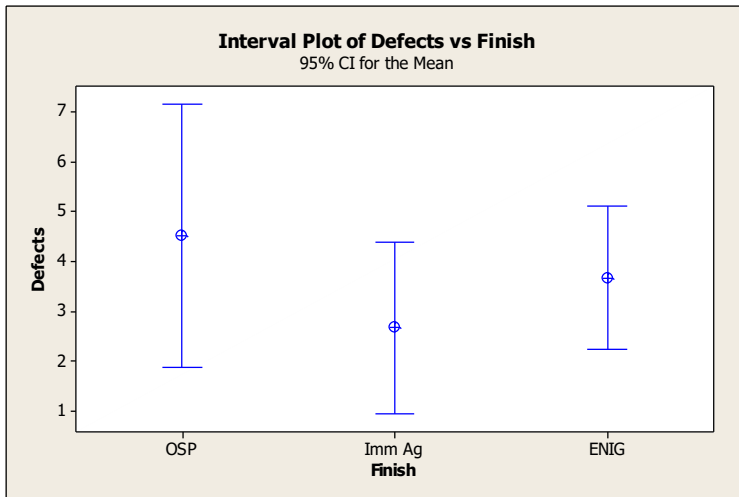Figure 8 illustrates the 95% confidence interval for each of the three board surface finishes.

Figure 8. Interval Plot of Defects vs. Finish.

Figure 9 illustrates the 95% confidence interval for each of the two stencil types.
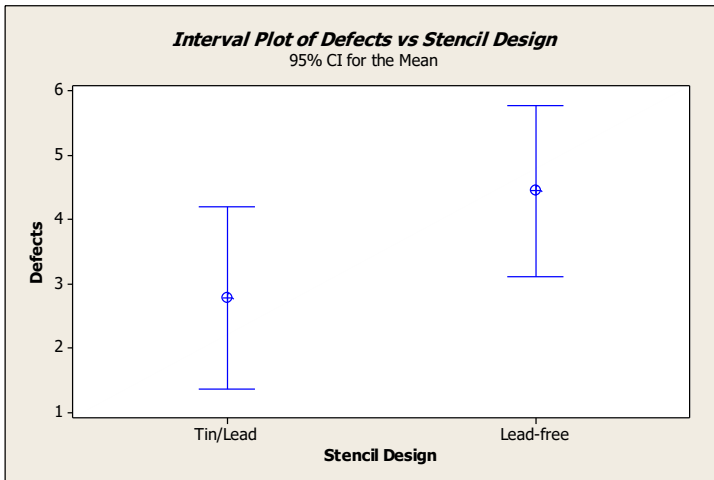
Figure 9. Interval Plot of Defects vs. Stencil Design

Comparison between Tin/Lead and Lead-free Process

To conduct a comparison between the results for the tin/lead and lead-free process, two tin/lead work orders previously completed by Benchmark Electronics were randomly selected. Work order H40997 included 50 boards, and work order H40596 included 44 boards for a total of 94 tin/lead boards. These work orders were completed in 2004.

Table 4 lists some of the key data for the tin/lead and lead-free defects identified.

Table 4. Tin/Lead and Lead-Free Defects.

Parameter	Tin/Lead Process	Lead-free Process
Number of Boards	94	18
Number of Defects	379	65
Mean Defects Per Board	4.03	3.61
Median Defects Per Board	2.0	3.5
Standard Deviation	4.56	1.94
Variance	20.83	3.78
Range	0 - 17	1 - 7

Using normality tests, it can be stated with 95% confidence that the lead-free defect distribution is normal and the tin/lead defect distribution is not normal. Therefore, non-parametric tests were used to compare the medians and variances between the tin/lead and lead-free processes. This difference in distribution is illustrated in the following histograms (Figures 10 and 11)
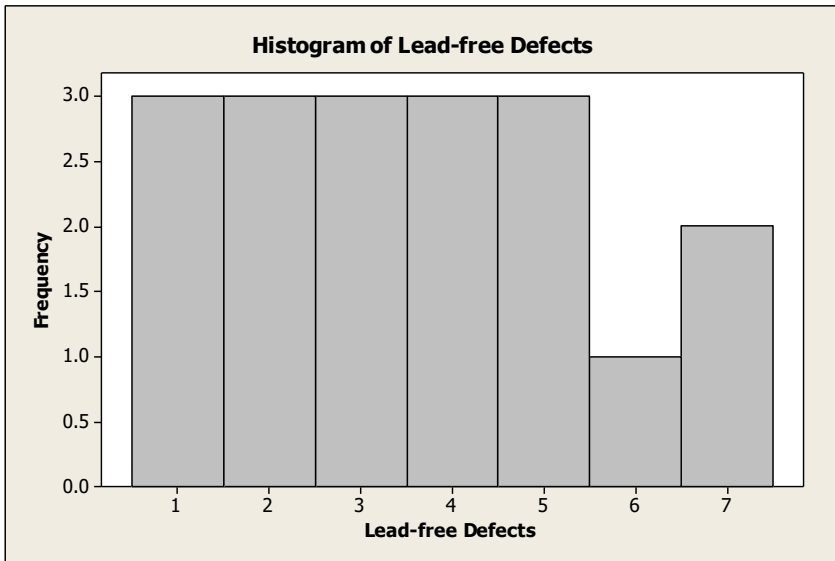
11

Figure 10. Histogram of Lead-free Defects.
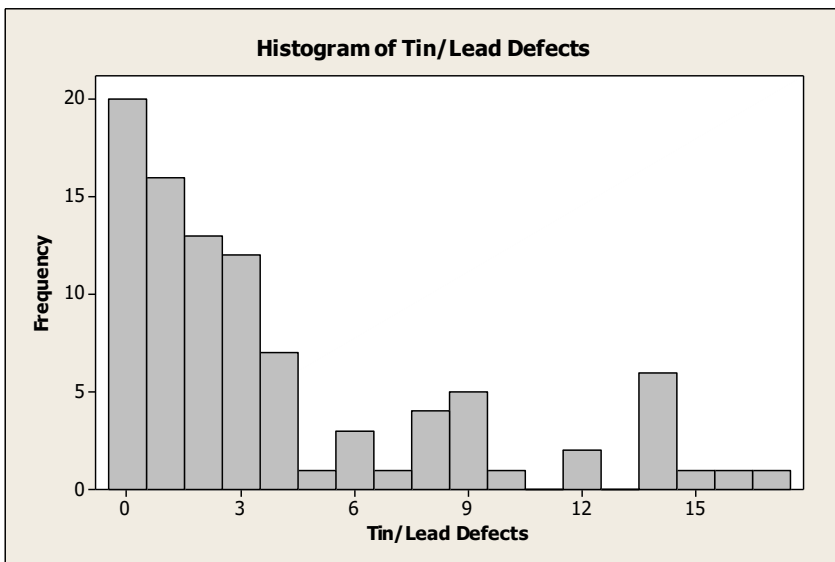
Figure 11. Histogram of Tin/Lead Defects.

Using a Mann-Whitney test, it can be stated with 95% confidence that there is not a difference between the median defects per board between the tin/lead and lead-free process. Further, by using a Levene's test, it can be stated with 95% confidence that there is not a difference between the variance of defects between the tin/lead and lead-free process.

The following Pareto chart (Figure 12) illustrates the types and quantity of defects identified during the test and inspection process for the 18 lead-free boards:

Occurrence of Lead-free Solder Related Defects

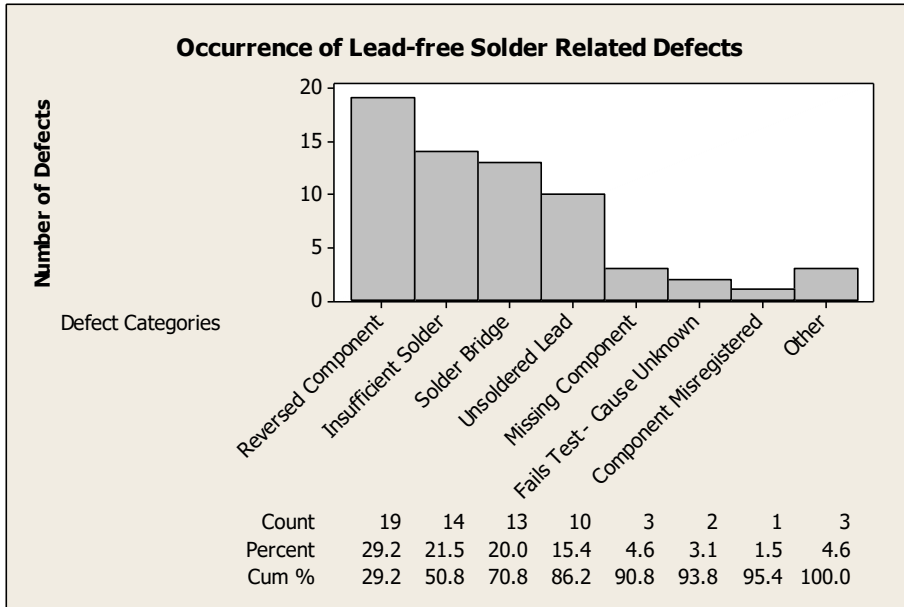|	Count	Percent	Cum %
Reversed Component	19	29.2	29.2
Insufficient Solder	14	21.5	50.8
Solder Bridge	13	20.0	70.8
Unsoldered Lead	10	15.4	86.2
Missing Component	3	4.6	90.8
Fails Test - Cause Unknown	2	3.1	93.8
Component Misregistered	1	1.5	95.4
Other	3	4.6	100.0

Figure 12. Occurrence of Lead-free Solder Related Defects.

The following Pareto chart (Figure 13) illustrates the types and quantity of defects identified during the test and inspection process for the 94 tin/lead boards assembled under work orders H40997 and H40596:

Occurrence of Tin/Lead Defects

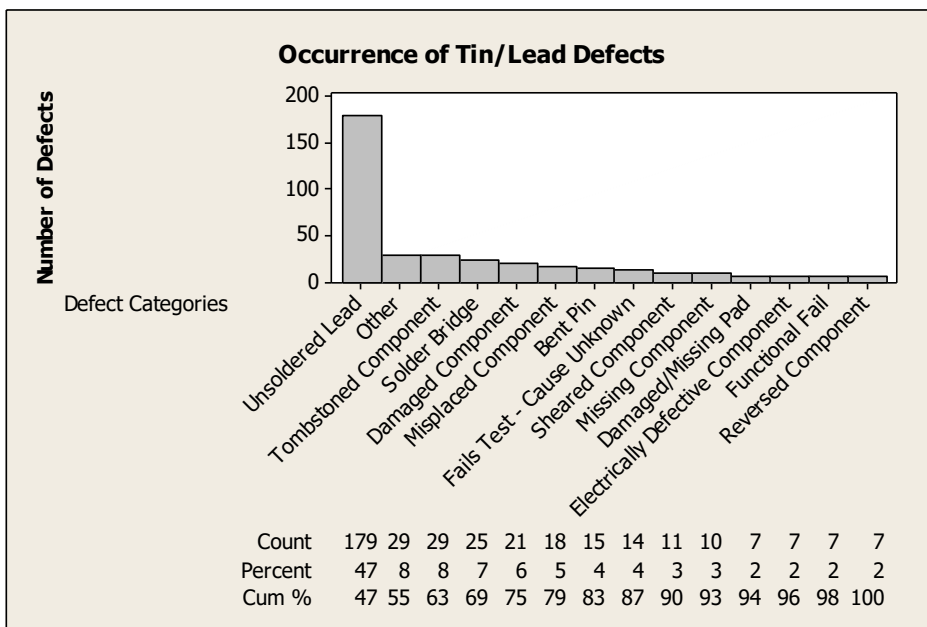|	Count	Percent	Cum %
Unsoldered Lead	179	47	47
Other	29	8	55
Tombstoned Component	29	8	63
Solder Bridge	25	7	69
Damaged Component	21	6	75
Misplaced Component	18	5	79
Bent Pin	15	4	83
Fails Test - Cause Unknown	14	4	87
Sheared Component	11	3	90
Missing Component	10	3	93
Damaged/Missing Pad	7	2	94
Electrically Defective Component	7	2	96
Functional Fail	7	2	98
Reversed Component	7	2	100

Figure 13. Occurrence of Tin/Lead Defects.

When evaluating the defects identified, one should consider that there are some defect categories related to manufacturing process issues and other defect categories related to soldering issues. This consideration will be further addressed in a subsequent section of this report.

Six Sigma Metrics

Three common process performance metrics used are Defects per Unit (DPU), Defects per Million Opportunities (DPMO), and sigma level.

Defects per Unit (DPU):
DPU is the total number of defects identified on all units divided by the number of units.

Defects per Million Opportunities (DPMO):
In order to calculate the number of opportunities, it is necessary to determine the number of ways a defect can occur on each item. An opportunity for defect could occur for each lead of a component, as well as for placing the correct component in the correct manner. For example, a component with eight leads would have 10 opportunities for defects (8 lead level + 2 component level). The total number of opportunities for defects for each board in this experiment is calculated to be 16,134.

Sigma Level:
Sigma level is used to describe the capability of a process to meet specification. A higher sigma level indicates that a process has a greater tendency for performing within its specification limits. A six sigma quality level is used to describe a process that has 3.4 defects per million opportunities.

Tin/Lead Board Assembly*:*
Boards (units): 94
Defects: 379

Defects per Unit (DPU) = 379/94 = 4.03

Defects per million opportunities (DPMO) = (379 * 1,000,000) / (94 * 16,134) = 249.9

Sigma Level = Approximately 5.0

Lead-free Board Assembly*:*
Boards (units): 18
Defects: 65

Defects per Unit (DPU) = 65/18 = 3.61

Defects per million opportunities (DPMO) = (65 * 1,000,000) / (18 * 16,134) = 223.8

Sigma Level = Approximately 5.0

Solder Paste Related Defects

The above analysis and metrics were based on total defects identified during the testing and inspection process. This includes defects that are manufacturing-assembly related as well defects that are soldering related. For this section, an analysis will be conducted for soldering related defects only. The manufacturing assembly related defects will be excluded from this analysis.

For the purposes of this report, the defect categories considered to be related to manufacturing assembly issues include: reversed component, missing component, bent pin, misplaced component, electrically defective component, damaged component, and sheared component. The defect categories that are considered to be related to soldering issues include: solder bridge, unsoldered lead, tombstoned component, nonwetting, and insufficient solder.

Table 4 illustrates the factorial design, as well as the number of solder-paste related defects identified during the testing and inspection process for the 18 lead-free boards.

Table 4. Factoral Design and Solder-Paste Related Defects

Board Number	Surface Finish	Stencil	Solder Paste Related Defects
1	OSP	Tin/Lead	4
2	OSP	Tin/Lead	0
3	OSP	Tin/Lead	0
4	OSP	Lead-free	2
5	OSP	Lead-free	4
6	OSP	Lead-free	4
7	Imm. Ag	Tin/Lead	0
8	Imm. Ag	Tin/Lead	1
9	Imm. Ag	Tin/Lead	2
10	Imm. Ag	Lead-free	0
11	Imm. Ag	Lead-free	2
12	Imm. Ag	Lead-free	4
13	ENIG	Tin/Lead	2
14	ENIG	Tin/Lead	1
15	ENIG	Tin/Lead	3
16	ENIG	Lead-free	4
17	ENIG	Lead-free	3
18	ENIG	Lead-free	2

Figure 14 illustrates the mean defect level per board for the three board surface finishes, and the two stencil types.
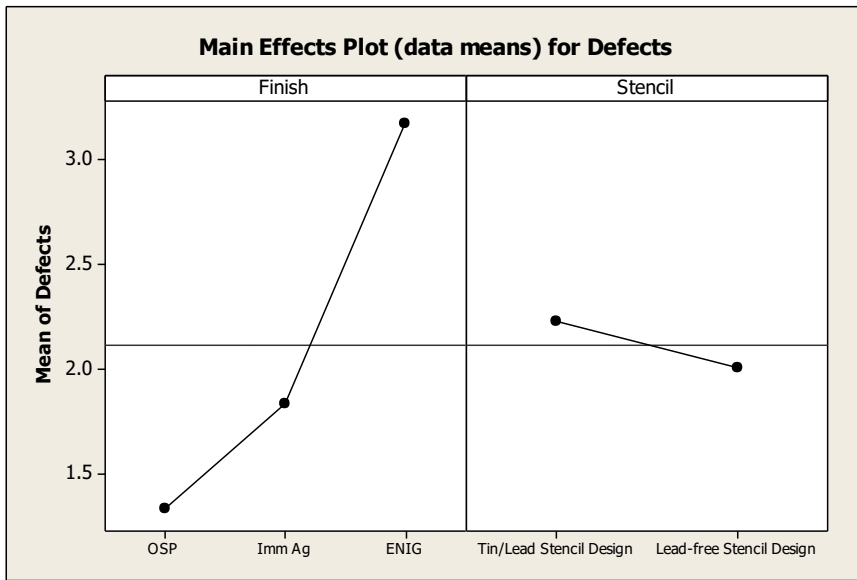
Figure 14. Main Effects Plot for Defects

The Analysis of Variance for Defects, using Adjusted Sum of Squares for Tests was used for analyzing the soldering-related defects. Since the probability is greater than 0.05 for the surface finish, stencil, and interaction effect, the null hypothesis should not be rejected. In other words, there is no statistical difference between the quantity of defects found between the boards based on board surface finish, stencil design, or any interactions of these two factors.

Table 5 lists some of the key data for the tin/lead and lead-free defects identified.

Table 5. Data for Tin/Lead and Lead-free Defects.

Parameter	Tin/Lead Process	Lead-free Process
Number of Boards	94	18
Number of Defects	241	38
Mean Defects Per Board	2.56	2.11
Median Defects Per Board	1.0	2.0
Standard Deviation	3.80	1.53
Variance	14.42	2.34
Range	0 - 4	0 - 14

Using a Mann-Whitney test, it can be stated with 95% confidence that there is not a difference between the median defects per board between the tin/lead and lead-free process. Further, by using a Levene's test, it can be stated with 95% confidence that there is not a difference between the variance of defects between the tin/lead and lead-free process.

The following Pareto chart (Figure 15) illustrates the types and quantity of soldering related defects identified during the test and inspection process for the eighteen lead-free boards.

Occurrence of Lead-free Solder Related Defects

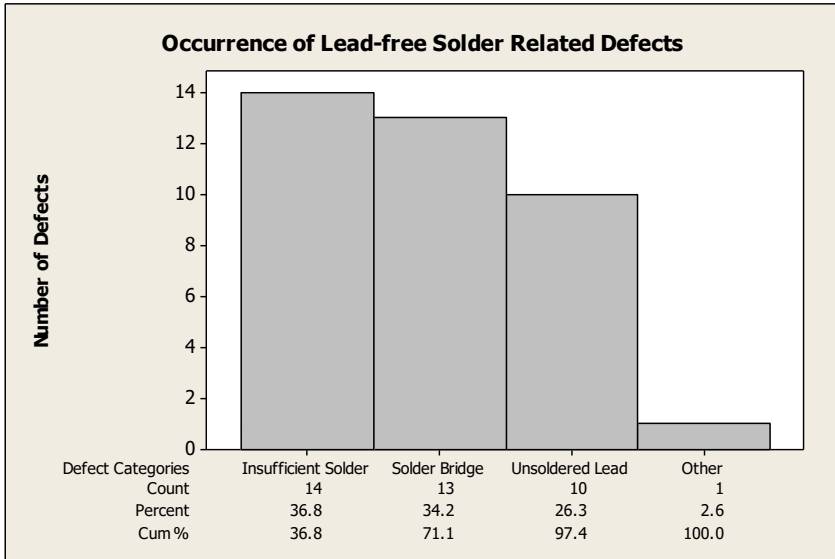| Defect Categories	Insufficient Solder	Solder Bridge	Unsoldered Lead	Other
Count	14	13	10	1
Percent	36.8	34.2	26.3	2.6
Cum %	36.8	71.1	97.4	100.0

Figure 15. Occurrence of Lead-free Solder Related Defects

The following Pareto chart (Figure 16) illustrates the types and quantity of soldering related defects identified during the test and inspection process for the 94 tin/lead boards assembled under work orders H40997 and H40596:
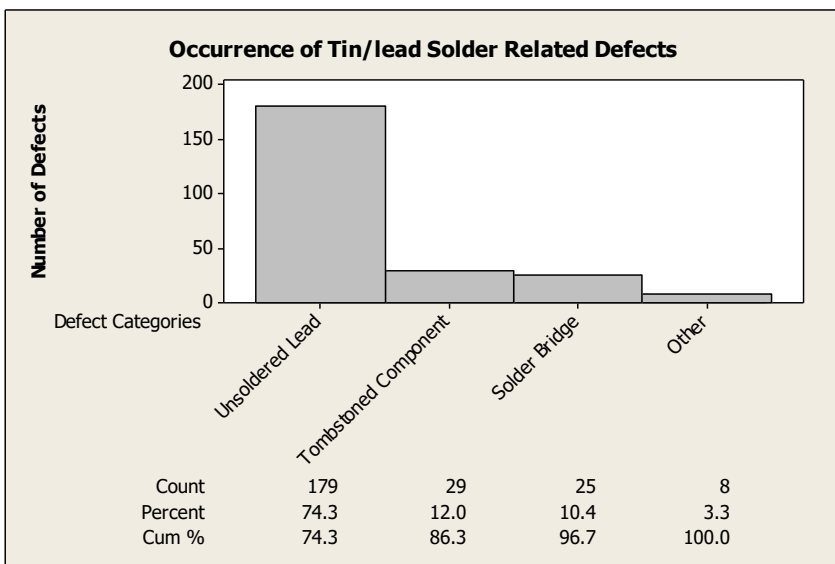
Occurrence of Tin/lead Solder Related Defects

Defect Categories	Unsoldered Lead	Tombstoned Component	Solder Bridge	Other
Count	179	29	25	8
Percent	74.3	12.0	10.4	3.3
Cum %	74.3	86.3	96.7	100.0

Figure 16. Occurrence of Tin/Lead Solder Related Defects.

Conclusions & Recommendations

The mean defect level for the lead-free assembly process is not influenced by the three board surface finishes or the two stencil designs used for this case study. Further, it can be stated with 95% confidence that there is no difference between the median defects per board or variance between the tin/lead and lead-free process. These conclusions are consistent for the analysis of the total defects, as well as the analysis for solder- related defects only.

Key Lessons Learned
1. Create a proper baseline of tin/lead process performance and quality metrics. This will be critical to compare the process and quality results for the new lead-free electronics assembly process.
2. Conduct careful selection of materials such as board laminate, board surface finish, and solder paste.
3. Carefully select processing parameters such as print speed and reflow profile.
4. Check for potential lot-to-lot variation of solder paste.
5. Determine availability of lead-free compatible components. The components should have a lead-free finish and the ability to withstand the higher temperature profile associated with lead-free electronics assembly.
6. Modify assembly process to accommodate components that are not lead-free compatible.
7. Conduct an X-ray fluorescence (XRF) scan of key materials and inputs (e.g. solder paste, components, board, hardware, and finished assembly) to ensure the end-product is RoHS compliant. XRF scans can be conducted during incoming inspection, inventory retrieval, in-process, or final inspection.
8. Conduct reliability testing of lead-free electronics solder joints as necessary for the particular application.